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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/081,338	02/22/2002	Jia-Fam Wong	B-4506 619547-1	9829

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EXAMINER	
DI GRAZIO, JEANNE A	
ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 06/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Applicati n No.	Applicant(s)	
	10/081,338	WONG, JIA-FAM	
	Examiner	Art Unit	
	Jeanne A. Di Grazio	2871	

-- The MAILING DATE of this communication appears on the cover sh et with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *RCE February 23, 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

Priority to Taiwan Patent Application No. 90107642 (March 30, 2001) is claimed.

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 7 and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by United States Patent 4,470,667 (to Okubo et al.).

As to claim 7, Okubo has, with reference to at least Figures 11 and 12 of a single embodiment, glass substrates (7 and "S"), a plurality of source lines (3, 3', and 3'')(Applicant's "signal lines") disposed on the glass substrate in a first direction and a plurality of gate lines (1a, 1a', and 1a'') disposed on the glass substrate along a second direction to define a plurality of elemental electrodes (4 and 4')(Applicant's "pixels"), the first direction being perpendicular to the second direction (Figure 11), each elemental electrode (pixel) including a first area (hatched regions of Figure 11), a plurality of TFTs (Applicant's "switching units")(TFTs 2, 2', 2'', 2''') disposed in the first areas of the pixels, a first color photoresist layer covering a first group of the elemental electrodes (color layer 110), a second color photoresist layer covering a second group of the elemental electrodes (color layer 111), a third color photoresist layer covering a third group of the elemental electrodes (color layer 112), wherein the first area of each elemental electrode is covered by at least two of the first, second, and third color photoresist layers (Figures 11 and 12).

As to claim 13, Okubo has, with reference to at least Figures 11 and 12 of a single embodiment, glass substrates (7 and "S"), a liquid crystal layer (11) disposed between the first ("S") and second (7) substrates, a plurality of source lines (3, 3', and 3'')(Applicant's "signal lines") disposed on the glass substrate in a first direction and a plurality of gate lines (1a, 1a', and 1a'') disposed on the glass substrate along a second direction to define a plurality of elemental electrodes (4 and 4')(Applicant's "pixels"), the first direction being perpendicular to the second direction (Figure 11), each elemental electrode (pixel) including a first area (hatched regions of Figure 11), a plurality of TFTs (Applicant's "switching units")(TFTs 2, 2', 2'', 2''') disposed in the first areas of the pixels, a first color photoresist layer covering a first group of the elemental electrodes (color layer 110), a second color photoresist layer covering a second group of the elemental electrodes (color layer 111), a third color photoresist layer covering a third group of the elemental electrodes (color layer 112), wherein the first areas of each elemental electrode is covered by at least two of the first, second, and third color photoresist layers (Figures 11 and 12).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-6, 8-12 and 14-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over United States Patent 4,470,667 (to Okubo et al.) in view of United States Patent 6,043,145 (to Suzuki et al.).

As to claims 1-6, the method steps forming on a substrate a plurality of source lines (3, 3', and 3'')(Applicant's "signal lines") disposed on the glass substrate in a first direction and a plurality of gate lines (1a, 1a', and 1a'') disposed on the glass substrate along a second direction to define a plurality of elemental electrodes (4 and 4')(Applicant's "pixels"), the first direction being perpendicular to the second direction (Figure 11), each elemental electrode (pixel) including a first area (hatched regions of Figure 11), forming a plurality of TFTs (Applicant's "switching units")(TFTs 2, 2', 2'', 2''') disposed in the first areas of the pixels, forming a first color photoresist layer covering a first group of the elemental electrodes (color layer 110), forming a second color photoresist layer covering a second group of the elemental electrodes (color layer 111), forming a third color photoresist layer covering a third group of the elemental electrodes (color layer 112), wherein the first area of each elemental electrode is covered by at least two of the first, second, and third color photoresist layers (Figures 11 and 12) and other recited steps would have been obvious in view of the structures as disclosed and taught by Okubo and Suzuki (see rejections below pertaining to the structure).

As to claims 8 and 14, Okubo does not appear to explicitly specify a plurality of through holes in at least two of the first, second, and third photoresist layers so as to expose each drain electrode of each thin film transistor therein.

Suzuki teaches and discloses a method for making a multi-layer wiring structure (Title, entire patent), and as can be seen in at least Figure 5D, illustrates at least a through hole that

pierces through three insulating layers and the at least through hole exposes a section of a wiring pattern (62) as can also be seen in Figure 5D. The through hole exposes a lower layer wiring pattern (62) on a semiconductor substrate (61) for reduced etching processes and improved yield (Column 16, Lines 13-21). So why is it obvious?

As to claims 9, 12, 15, and 18, Okubo does not appear to explicitly specify a conducting layer on first, second, and third photoresist layers and connected to each drain electrode via corresponding through hole in the first area.

Suzuki teaches and discloses a method for making a multi-layer wiring structure (Title, entire patent) and discloses the depositing of a conductive material to cover the insulating films (Col. 14, Lines 60-64) contributing to improved fineness and precision (Column 16, Lines 30-33).

Suzuki is evidence that ordinary workers in the field of liquid crystals would have found the reason, suggestion, and motivation to include a conducting layer on photoresist layers at least to contribute to improved fineness and precision.

Therefore, it would have been obvious to one of ordinary skill in the art of liquid crystals at the time the invention was made to include a conductive layer to fill in connecting holes and to cover the insulating layers (Col. 14, Lines 60-64) and for improved fineness and precision.

As to claims 10 and 16, Okubo does not appear to explicitly specify a passivation layer formed between a first photoresist layer and each switching unit(s) in each first area.

Suzuki teaches and discloses a method for making a multi-layer wiring structure (Title, entire patent) and including the optional method of forming a protective film or the like between

a lower-layer wiring pattern and first insulating film (Col. 15, Lines 54-61) for the purpose of preventing contact between a lower-layer wiring pattern and a first insulating film (Id.).

Suzuki is evidence that ordinary workers in the field of liquid crystals would have found the reason, suggestion, and motivation to include a passivation layer between a photoresist and switching unit to prevent contact between the photoresist and switching unit.

Therefore, it would have been obvious to one of ordinary skill in the art of liquid crystals at the time the invention was made to include a passivation layer between switching units and first photoresist layer for preventing contact between the switching units and first photoresist layer (Id.).

As to claims 11 and 17, Because Suzuki discloses that a protective film may be formed between the lower-layer wiring pattern and first insulating film, and a through hole pierces through the three insulating layers as shown in Figure 5D, the through hole may also pierce through the protective film if so desired to facilitate connections to the wiring layer.

Therefore, it would have been obvious to one of ordinary skill in the art of liquid crystals at the time the invention was made to include a through hole through the photoresist layers and passivation film to facilitate connection to the wiring patterns as suggested by the teachings of Suzuki.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeanne A. Di Grazio whose telephone number is (571)272-2289. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim, can be reached on (571)272-2293. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jeanne Andrea Di Grazio

Patent Examiner
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